Notice of Allowability	Application No.	Applicant(s)	
	09/928,848	MANDELL ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *27 April 2005*.

2. ☒ The allowed claim(s) is/are *1-4,6 and 8-14 (now renumbered 1-12)*.

3. ☒ The drawings filed on *13 August 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *13 July 2005* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Amended independent claims 1,6 & 9 are currently pending in this application based on applicant's disclosure filed 27th April 2005.
2. Applicants have cancelled claims 5 & 7.
3. Claims 1, 6 & 9 have now been allowed over the prior art of record.
4. Claims 6 and 9 are allowed after examiner's amendment as discussed with applicant on 13th July 2005.

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Michael L Taylor on 13th July 2005.

Amend claim 6 with the following:

On page 5 of applicant's amendment filed on 27th April 2005, **delete** "and" after "circuit simulation;" and "." at end of claim 6. Further amend the claim 6 by **inserting** the words "; and computing an index for said marker component using the running count of time.", at the end. The amended claim should now read as follows (examiners amendment underlined):

6. (currently amended) A method of characterizing a circuit at a hardware level description, using a processor, comprising:
creating a behavioral level description of said circuit;
generating symbolic equations for components of said behavioral level description using the processor;
partitioning said behavioral level description using the processor by inserting a marker component into said behavioral level description to simplify subsequent processing used to prove equivalence of said behavioral and hardware level descriptions; and
defining said marker component using a unique symbolic name;
maintaining a running count of time during a circuit simulation; **[[and]]**
forming said behavioral Level description to include a descriptive netlist **[[.]]; and computing an index for said marker component using the running count of time.**

Amend claim 8 with the following:

Claim 8 is now amended as follows:

8. The method of claim **[[7]]** **6** further comprising:
generating an output string; and
printing said output string to equation file.

Amend claim 9 with the following:

On page 6 of applicant's amendment filed on 27th April 2005, **delete** "and" after "...circuit simulation;" and "." at end of claim 9. Further amend the claim 9 by **inserting** the words "; and computing an index for said marker component using the running count of time.", at the end. The amended claim should now read as follows (examiners amendment underlined):

9. (currently amended) A method of characterizing a circuit at a hardware level description, using a processor, comprising:
creating a behavioral level description of said circuit including a plurality of components;
partitioning said behavioral level description, using the processor, by inserting a marker component into said behavioral level description to simplify subsequent processing used to prove equivalence of said behavioral and hardware level descriptions and to create a modified behavioral level description;
constructing a symbolic hardware description language code from said modified behavioral level description using a processor;
forming a running count of time during a circuit simulation; **[[and]]**
forming said behavioral level description to include a descriptive netlist **[[.]]; and computing an index for said marker component using the running count of time.**

Information Disclosure Statement

6. Examiner withdraws objection under § 1.56 in view of applicant's amendment to incorporate by reference application no. 09/918596 (US Patent No. 6,757,884), filed 27th April 2005.

Claim Rejections - 35 USC § 101

7. Examiner withdraws *35 USC § 101* rejections for claims 1-4, 6-14 in view of applicant's amendment to claims 1-4, 6-14, filed 27th April 2005.

Claim Rejections - 35 USC § 112

8. Examiner withdraws *35 USC § 112* rejections for claims 1-4, 6-14 in view of applicant's amendment to claims 1-4, 6-14, filed 27th April 2005.

Claim Rejections - 35 USC § 103

9. Applicant's arguments filed 27th April 2005 with respect to claims 1, 6 and 9 have been fully considered and are persuasive. The 103(a) rejections have been withdrawn in view of applicant's amendment to the claims and cancellation of claims 5 & 7.

Allowable Subject Matter

10. Claims 1,6 and 9 have now been allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing a method of characterizing a circuit at a hardware level description including the steps of creating behavioral level description, generating symbolic equations for behavioral level description and partitioning behavioral level description using a computer by inserting markers into the behavioral level description, where the index of the marker is computed using current time counts of each clock cycle. The step of partitioning is used to simplify the subsequent processing used to provide equivalence between the behavioral and hardware level description (RTL netlist). The individual steps of creating, generating, partitioning and defining a marker with time index have been disclosed in prior art of record. Specifically, such features are generally available in commercial software products like Behavioral Compiler by Synopsys and articles by Michael C McFarland, S.J., Chaiyakul & Gajski, .

While these features are individually disclosed in the prior art, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

In particular, the prior art of record does not disclose inserting a marker component, indexed with running count of time from simulation clock, during partitioning of symbolic equations representing the behavioral level description as now recited in independent claims 1,6, and 9. (See: Specification Pg.15 ¶0053 Pg.17 ¶0057,0058; Pg.18¶0059,0060; Fig.17 & 18).

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

U.S. Patent 5,933,356 issued to Rostoker: Rostoker teaches an electronic design (circuit) can be described using a behavioral level description (Rostoker: Col. 32 Line 31-35), which can further described inform of symbolic form (Rostoker: Col. 26 Line 56-60). He further discloses that behavioral design can be partitioned into number of blocks (Rostoker: Col. 32 Line 38-40) to meet the equivalence between the structural (hardware level description) and behavioral description (Rostoker: Col. 26 Line 48-50). However, Rostoker does not state the use of a marker in partitioning the design as now recited in independent claims 1,6 & 9.

Synopsys articles No. 901157, 002613, 901665, 901336, and 901884: Synopsys article (Doc Id 901157) teaches a concept, similar in function of a marker, using

compiler directives (Doc Id: 002613) in Behavioral Compiler, a Synopsys product. This article teaches how compiler directives "preserved_function" is used to set aside a section of code and implement it as described, essentially partitioning it from the rest of the code and reducing complexity. The "preserved_function" compiler directive is known to exist in 1998 (Doc Id: 901665). Also "partition_dp" (Doc Id: 901336) command can be used to do partitioning at behavioral level. The command marker disclosed has a unique symbolic name, as multiple compiler directives can be present in a single program. The "case" construct example (Doc Id 901157) demonstrates that multiple compiler directives can be used in the same code. It is understood that compiler will internally know how to distinguish them, hence will uniquely identify them. However, Synopsys does not disclose or render obvious the limitation relating to insertion of a *time indexed marker* component during partitioning of symbolic equations representing the behavioral level description, as now recited in independent claims 1,6, and 9.

Article *"Computer-Aided Partitioning of Behavioral Hardware Descriptions"* by Michael C McFarland, S.J., sites the concerns related to partitioning a behavioral model in the absence of data paths allocations and basis of such partitioning. He further describes metrics, qualitative & quantitative analysis between methods of partitioning and equivalence.

Article "*Assignment Decision Diagram for High Level Synthesis*" by Chaiyakul & Gajski, details how a behavioral description can be represented in partially unique hardware descriptive language (HDL), irrespective of way the description is

provided. It details how different constructs implied in the behavioral description are transformed/synthesized into HDL through decomposition. This decomposition has intermediate marker like characteristics described by the inventor.

Further, updated searches revealed a new article, but it neither discloses nor renders obvious the limitation relating to time indexing the marker component during partitioning of symbolic equations representing the behavioral level description.

Article "*Hierarchical Model Partitioning for parallel VLSI-Simulation using Evolutionary Algorithms improved by super-positions of partitions*" by R. Haupt et al (Haupt hereafter), teaches a scheme of partitioning the design as structural hardware model (SHM) as bipartite graph, which closely resembles the marker makeup disclosed by the applicant (See: Specification Pg.12 ¶0047; Pg.12 Table 1; Fig.17 & 18). Further, there is a strong suggestion of using time (single clock cycle) (Haupt: Pg.2 Section 1.2 & Footnote) as a simulation basis to minimize the partition dependent runtime. However, Haupt does not disclose or render obvious the limitation relating to insertion of a *time indexed marker* component during partitioning of symbolic equations representing the behavioral level description,

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled **"Comments on Statement of Reasons for Allowance."**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Wednesday, July 13, 2005

JEAN R. HOMERE
PRIMARY EXAMINER